REMARKS

The Office Action dated June 1, 2005, has been received and reviewed.

Claims 1-22 are currently pending and under consideration in the above-referenced application. Each of claims 1-22 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

35 U.S.C. § 112 Claim Rejections

Claims 13-17 stand rejected under 35 U.S.C. § 112, second paragraph, for reciting subject matter which is purportedly indefinite.

Claim 13 is directed to an assembly method that includes positioning at least two first-level semiconductor devices within a receptacle of an interposer. At least one of the first-level semiconductor devices is positioned in the receptacle such that a backside thereof is substantially coplanar with a surface of the interposer substrate, or located within a plane that extends through the substrate. *See* independent claim 1. Another first-level semiconductor device is also positioned within the receptacle, with its backside facing the backside of the aforementioned first-level semiconductor device. *See* claim 13.

It has been asserted that use of the term "first-level" in describing the semiconductor device of claim 13 is confusing, as the two or more semiconductor devices would not be located in a single plane, or at a single elevation. The only source for such confusion is the Office's narrow reading of the term "level," which should not be limited to location of an element in a particular plane or at a particular elevation.

As one of ordinary skill in the art would readily understand from reading claim 13 that the term "level," as used in claims 1 and 13, does not refer to the plane in which a "first-level" semiconductor device is located, it is respectfully submitted that one of ordinary skill in the art would be readily apprised of the scope of claim 13. Therefore, claim 13 complies with the definiteness requirement of 35 U.S.C. § 112, second paragraph.

Claims 14-17 were rejected merely for depending from claim 13.

Withdrawal of the 35 U.S.C. § 112, second paragraph, rejection of claims 13-17 is respectfully requested.

Rejections Under 35 U.S.C. § 102

Claims 1-12 and 18-22 have been rejected under 35 U.S.C. § 102.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Independent claim 1 recites a method for assembling a multi-die semiconductor device package. The method of independent claim 1 includes, among other things, positioning at least one first-level semiconductor device in a receptacle of an interposer. A backside of the at least one first-level semiconductor device is substantially coplanar with a surface of a substrate of the interposer, or located in a plane that extends through the substrate. The method of independent claim 1 also includes electrically connecting the at least one first-level semiconductor device to a conductor on an upper surface of the interposer substrate by way of a conductive member that is at least partially carried by the upper surface of the substrate or a second-level semiconductor device, or electrically connecting the first-level semiconductor device to a second-level semiconductor device.

In addition, the method of independent claim 1, as amended and presented herein, includes positioning the second-level semiconductor device above an upper surface of the substrate, with at least a portion of the second-level semiconductor device being superimposed with the upper surface.

The method recited in independent claim 18 includes positioning a first semiconductor device over a first surface of an interposer and positioning a second semiconductor device over a second surface of the interposer.

Washida

Claims 1, 5-8, and 18-21 stand rejected under 35 U.S.C. § 102(b) for reciting subject matter which is purportedly anticipated by the subject matter described in U.S. Patent 5,949,135 to Washida et al. (hereinafter "Washida").

Washida describes semiconductor device assembly methods in which a first semiconductor device 760, 860 is positioned with a hole 701a, 801a of a substrate 700, 800. That semiconductor device 760, 860 is electrically connected, in a flip-chip fashion, to a second semiconductor device 750, 850, which is positioned over the hole 701a, 801a.

Although Washida discloses positioning the second semiconductor device 750, 850 above an upper surface of the substrate 701, 801, Washida does not expressly or inherently describe positioning the second semiconductor device 750, 850 such that it is superimposed with a surface of the substrate 701, 801.

Therefore, Washida does not anticipate each and every element of amended independent claim 1, as would be required to maintain the 35 U.S.C. § 102(b) rejection of independent claim 1.

Each of claims 5-8 is allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 5 is additionally allowable since Washida lacks any express or inherent description of forming or positioning intermediate conductive elements between bond pads of the first semiconductor device 760, 860 and corresponding contacts 706, 806 of the substrate 701, 801.

With respect to the subject matter recited in independent claim 18, Washida includes no express or inherent description of positioning first and second semiconductor devices *over* the surfaces of an interposer. While Washida describes positioning a semiconductor device 750, 850 over one surface of a substrate 701, 801, Washida does not expressly or inherently describe that another semiconductor device 760, 860 is positioned over another surface of the substrate 701, 801. Rather than being positioned over a surface of the interposer, that semiconductor device 760, 860 is positioned at least partially within a hole 701a, 801a that extends through a

substrate 701, 801. Therefore, Washida does not anticipate each and every element of independent claim 18.

Claims 19-21 are each allowable, among other reasons, for depending directly or indirectly from claim 18, which is allowable.

Shimada

Claims 1-6 stand rejected under 35 U.S.C. § 102(e) for being drawn to subject matter that is allegedly anticipated by the subject matter described in U.S. Patent 6,365,963 to Shimada (hereinafter "Shimada").

The disclosure of Shimada relates to assembly methods that include positioning a first chip 11 within an opening 102 of a rigid board 101. FIG. 3; col. 3, lines 1-9. The first chip 11 is electrically connected to a base film 110 located adjacent to a bottom surface of the rigid board 101. FIG. 3; col. 3, lines 26-33. A second chip 12 is positioned over an upper surface of the rigid board 101 and electrically connected to electrode pads 105 on the upper surface of the rigid board 101. FIG. 3; col. 3, lines 41-45.

Shimada includes no express or inherent description of electrically connecting the first chip 11 to electrode pads 105 on the upper surface of the rigid board 101(*i.e.*, the surface of the rigid board 101 over which the second chip 12 is positioned) by way of a conductive member that is at least partially carried by the upper surface of the rigid board 101 or the second chip 12. Shimada also lacks any express or inherent description of electrically connecting the first chip 11 to the second chip 12. Therefore, Shimada does not expressly or inherently describe "electrically connecting . . . at least one first-level semiconductor device," which is positioned within a receptacle of a substrate of an interposer, to "conductors on the upper surface of the substrate by first-level conductive members that are at least partially carried by at least one of the upper surface and [a] second-level semiconductor device" or electrically connecting the at least one first-level semiconductor device to a second-level semiconductor device. As such, Shimada does not anticipate each and every element of amended independent claim 1.

Therefore, under 35 U.S.C. § 102(e), the subject matter to which independent claim 1 is drawn is allowable over the subject matter disclosed in Shimada.

Claims 2-6 are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowalble.

Claim 5 is further allowable since Shimada does not expressly or inherently describe forming or positioning intermediate conductive elements between bond pads of a first-level semiconductor device and corresponding conductors on an upper surface of an interposer substrate. Instead, the description of Shimada is limited to forming or positioning bond wires 114 between the bond pads of a first chip 11 and corresponding electrode pads 112 of a base film 110. The circuit traces of the base film 110 and conductive vias 104 of the interposer do not fall within the scope and meaning of the "intermediate conductive elements" recited in claim 5.

DiCaprio

Claims 1-6 and 9-12 are rejected under 35 U.S.C. § 102(e) for being directed to subject matter that is assertedly anticipated by the disclosure of U.S. Patent 6,452,278 to DiCaprio et al. (hereinafter "DiCaprio").

DiCaprio describes an assembly process that includes positioning a first die 12 within an aperture 15 of a substrate 14, positioning a second die 50 over the first die 12 and an upper surface of the substrate 14, and electrically connecting the first and second dice 12 and 50 to conductors (metal layers 16) on the upper surface of the substrate 14. FIGs. 3 and 4; col. 2, lines 24-58; col. 3, lines 26-46.

While DiCaprio describes that a second die 50 may be positioned above an upper surface of the substrate 14, DiCaprio lacks any express or inherent description of positioning the second die 50 so as to superimpose the same with a surface of the substrate 701, 801.

Therefore, Washida does not anticipate each and every element of amended independent claim 1, as would be required to maintain the 35 U.S.C. § 102(b) rejection of independent claim 1.

Each of claims 2-6 and 9-12 is allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Oka

Claims 18, 19, 21, and 22 have been rejected under 35 U.S.C. § 102(e) for reciting subject matter that is purportedly anticipated by the subject matter described in U.S. Patent 6,441,495 to Oka et al. (hereinafter "Oka").

The description of Oka relates to processes for securing leads to semiconductor devices. One of these processes is a so-called "tape-automated bonding" (TAB) process, in which the leads are carried by a polymeric film (*i.e.,* tape). This processes, shown in FIGs. 17 and 18 of Oka and described at col. 13, line 11, to col. 14, line 38 thereof, includes providing a TAB substrate, which, again, essentially includes leads carried by tape.

As those of ordinary skill in the art are aware, a TAB substrate is not an interposer. Therefore, Oka lacks any express or inherent description of "providing an interposer," as would be required to anticipate each and every element of independent claim 18. Therefore, under 35 U.S.C. § 102(e), the subject matter recited in independent claim 18 is allowable over the subject matter described in Oka.

Claims 19, 21, and 22 are each allowable, among other reasons, for depending directly or indirectly from claim 18, which is allowable.

Urushima

Claims 1, 7, and 8 stand rejected under 35 U.S.C. § 102(e) for being directed to subject matter which is purportedly anticipated by the disclosure of U.S. Patent 6,791,195 to Urushima et al. (hereinafter "Urushima").

FIG. 11A of Urushima illustrates an assembly that may be formed by positioning a first-level semiconductor device 3d in a hole 51 formed through an interposer 48, positioning two second-level semiconductor devices 3c and 3e over the first-level semiconductor device 3d and portions of an upper surface of the interposer 48, electrically connecting the first-level semiconductor device 3d to the second-level semiconductor devices 3c and 3e, and electrically connecting the second-level semiconductor devices to conductors on the upper surface of the interposer 48. *See also* col. 20, lines 5-56.

Urushima does not expressly or inherently describe positioning the first-level semiconductor device 3d such that a backside thereof is substantially coplanar with a surface of the interposer 48 or is located within a plane that extends through the interposer 48. Instead, as FIG. 11A clearly depicts, the backside of the first-level semiconductor device 3d described in Urushima is located in a plane beneath the interposer 48. Therefore, Urushima does not anticipate each and every element of independent claim 1 under 35 U.S.C. § 102(e).

Claims 7 and 8 are both allowable, among other reasons, for depending respectively directly and indirectly from claim 1, which is allowable.

It is respectfully requested that the 35 U.S.C. § 102 rejections of claims 1-12 and 18-22 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Each of claims 13-17 is rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Urushima in View of Morinaga

Claims 13 and 14 have been rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is assertedly unpatentable over the subject matter taught in Urushima, in view of the teachings of U.S. Patent Application Publication 2002/0047214 to Morinaga et al. (hereinafter "Morinaga").

Claims 13 and 14 are both allowable, among other reasons, for respectively depending directly and indirectly from claim 1, which is allowable.

Moreover, one of ordinary skill in the art would have no reason to expect that the asserted combination of reference teachings would successfully result in the method recited in claim 13 or claim 14. This is because the teachings of Urushima are limited to assembling a first-level semiconductor device 3d with an interposer 48 so that a backside of the semiconductor device 3d is located outside of a plane of the interposer 48. Thus, any additional first-level semiconductor device assemblied therewith could not be located within the hole 51 that extends through the interposer 48. As such, it is respectfully submitted that a *prima facie* case of obviousness has not been established against claim 13 or claim 14, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims..

Urushima, Morinaga, and Taniguchi

Claims 15-17 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over teachings from Urushima, in view of the subject matter taught in Morinaga and, further, in view of the teachings of U.S. Patent 6,388,333 to Taniguchi et al. (hereinafter "Taniguchi").

Claims 15-17 are each allowable, among other reasons, for depending indirectly from claim 1, which is allowable.

DiCaprio in View of Morinaga

Claims 13 and 14 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over DiCaprio et al. in view of Morinaga et al.

Both claim 13 and claim 14 are allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

DiCaprio, Morinaga, and Taniguchi

Claims 15-17 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over DiCaprio et al. in view of Morinaga et al., as applied to claim 13 above, and further in view of Taniguchi et al.

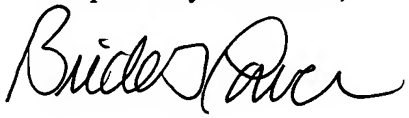
Each of claims 15-17 is allowable, among other reasons, for depending indirectly from claim 1, which is allowable.

Withdrawal of the 35 U.S.C. § 103(a) rejections of claims 13-17 is respectfully requested.

CONCLUSION

It is respectfully submitted that each of claims 1-22 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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